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**REMARKS**

By the present amendment and response, claims 1, 12, 23, 58, 70, and 71 have been amended to overcome the Examiner's objections. Claims 1-34 and 58-71 are pending in the present application. Reconsideration and allowance of pending claims 1-34 and 58-71 in view of the following remarks are requested.

The Examiner has rejected claims 1-34 and 58-71 under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has amended independent claims 1, 12, 23, 58, 70, and 71 to recite a pinned transfer gate being "tied" to a potential of a substrate. Applicant respectfully submits that support for this amendment is found at, for example, page 6, lines 12-25 to page 7, lines 1-10 of the present application.

In particular, pinned transfer gate 206 is formed from shallow p++ implanted pinned region 219 in an n-implanted transfer region 221 in p-type substrate 202. See, for example, page 6, lines 22-23 and Figure 2 of the present application. Thus, shallow p++ implanted pinned region 219 forms a connection with p-type substrate 202 and, thereby, with the potential of p-type substrate 202. However, since pinned transfer gate 206 is formed from shallow p++ implanted pinned region 219, pinned transfer gate 206 is "tied" to the potential of p-type substrate 202 by shallow p++ implanted pinned region 219.

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The Examiner has also rejected claims 1-34 and 58-71 under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Examiner has stated that “[i]t is not known in the art how to make and use a ‘Pinned Transfer Gate,’ nor has Applicant sufficiently explained how to do so.” Page 4 of the Office Action dated June 28, 2004. Applicant respectfully disagrees with the Examiner for the following reasons.

In U.S. patent number 5,077,592 to James R. Janesick (“Janesick”), for example, Janesick discloses an open pinned-phase pixel having an open-phase region including n-channel 10 having a shallow implant of p-type doping, which pins the surface potential to zero volts at the interface between thin oxide film 18 and n-channel 10 in the open phase region. See, for example, column 4, lines 39-49 and Figure 1 of Janesick. Thus, Janesick discloses how to “pin” the surface potential of an open phase region of an open pinned-phase pixel to zero volts by forming a shallow implant of p-type doping is formed in an n-channel. Thus, Applicant respectfully submits that the teachings of Janesick, as well as a variety of other references disclosing and teaching “pinned photodiodes,” can be used by one of ordinary skill in the art to manufacture the pinned transfer gate disclosed in the present application. Accordingly, Applicant respectfully submits that the requirements of 35 USC §112, first paragraph, have been met.

The Examiner has rejected claims 1 and 5-8 under 35 USC §102(e) as being anticipated by U.S. patent number 6,603,144 B2 to Shiro Tsunai (“Tsunai”). For the

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reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Tsunai.

The present invention, as defined by amended independent claim 1, teaches, among other things, an imager cell including a pinned transfer gate configured to transfer charge between a photoreceptor and a sense node, "wherein a voltage determined by the charge transferred between the photoreceptor and the sense node is read out of the imager cell at the sense node." As disclosed in the present application, a "pinned transfer gate" is tied to the same voltage or potential as the substrate. See, for example, page 7, lines 6-7 of the present application. By utilizing a pinned transfer gate to transfer charge between a photoreceptor and a sense node, the present invention advantageously achieves an imager cell that does not require a transistor gate structure, which is conventionally used to transfer charge from the photoreceptor to the sense node.

As disclosed in the present application, photons incident on the photoreceptor produce electrons that are captured in an integration potential well, which is established by an integration voltage  $V_+$ . As further disclosed in the present application, after the integration period, a readout potential well is established, which is shallower than the transfer potential established by the pinned transfer gate. As a result, electrons captured by the integration potential well propagate through the transfer potential well into the sense node potential well, where they (i.e. the electrons) can be read. As disclosed in the present application, a source follower can be used to amplify and buffer the resultant potential at the sense node onto a column bus. Thus, by employing a pinned transfer gate

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situated between a photoreceptor and a sense node, the present invention advantageously achieves the above readout operation without requiring a transistor gate structure.

In contrast, Tsunai does not teach, disclose, or suggest an imager cell including a pinned transfer gate configured to transfer charge between a photoreceptor and a sense node, "wherein a voltage determined by the charge transferred between the photoreceptor and the sense node is read out of the imager cell at the sense node." Tsunai is directed to a solid-state imaging device having an overflow drain, which prevents excessive electrons that cannot be accumulated in a photodiode from overflowing into the charge transfer elements or into adjacent pixels and causing undesirable flare and blooming. See, for example, Tsunai, column 3, lines 54-59. Tsunai specifically discloses photodiode N well 16 situated between charge transfer N well 14, which forms charge transfer element 8, and drain 5, which is used to drain off the electrical charge overflowing from photodiode N well 16. See, for example, column 4, lines 13-20 and Figure 2(a) of Tsunai. In Tsunai, drain 5 is connected to a power supply. See, for example, Tsunai, column 4, lines 22-23.

On page 6 of the Office Action dated June 28, 2004, the Examiner refers to drain 5 as "sense node 5." However, in Tsunai, drain 5 is connected to a power supply and used to drain off excessive electrical charge that is overflowing from photodiode N well 16 to prevent flare and blooming. As such, drain 5 is completely different than the sense node recited in amended independent claim 1, which is used to provide a voltage that can be read out of an imager cell. Thus, Tsunai fails to teach, disclose, or suggest an imager cell including a pinned transfer gate configured to transfer charge between a photoreceptor

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and a sense node, where a voltage determined by the charge transferred between the photoreceptor and the sense node is read out of the imager cell at the sense node.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Tsunai. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Tsunai. Thus claims 5-8 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Tsunai for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 2-34 and 58-71 under 35 USC §103(a) as being unpatentable over Tsunai. Applicant has amended independent claims 12, 23, 58, 70, and 71 to specify limitations analogous to those specified by amended independent claim 1. As discussed above, amended independent claim 1 is patentably distinguishable over Tsunai. Thus, for similar reasons as discussed above, amended independent claims 12, 23, 58, 70, and 71 are also patentably distinguishable over Tsunai and, as such, corresponding dependent claims 2-11, 13-22, 24-34, and 59-69 are, *a fortiori*, also patentably distinguishable over Tsunai for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 12, 23, 58, 70, and 71 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-34 and 58-

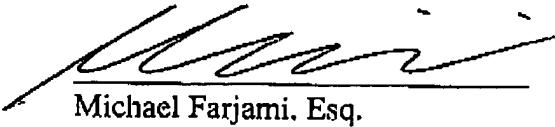
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71 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-34 and 58-71 pending in the present application is respectfully requested.

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Respectfully Submitted,  
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